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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,499	03/15/2004	Daniel Calafut	018865-015200US	1835

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,499	CALAFUT ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/1/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 1, 2006 has been entered.

Status of the Claims

2. Amendment filed September 1, 2006 has been entered. Claims 11 and 12 have been cancelled. Claims 1, 5-7 and 13 has been amended. Claims 14-18 have been added. Claims 1-10 and 13-18 are pending.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "the second trench including a conductive material coupled to the conductive material in the first trench" (claim 5) and "the conductive material in the first trench electrically connects to the conductive material in the pair of adjacent trenches between which the Schottky diode is formed" (claim 6), must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing

should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-10 and 13-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "wherein the Schottky consumes 0.5-4.5 % of the active area" (claims 1 and 13) in the application as filed.

The specification fails to provide support for the actual value of "0.5-4.5 %".

Applicant must cancel the new matter.

With respect to claims 5 and 6, there does not appear to be a written description of the claim limitation "a second trench adjacent to the first trench, the second trench including a conductive material coupled to the conductive material in the first trench" (claim 5) and "the conductive material in the *first trench* electrically connects to the conductive material in the pair of adjacent trenches between which the Schottky diode is formed" (claim 6)in the application as filed.

Note that each trench gate are independent from each other, e.g., no connection, and the conductive material in the pair of the adjacent trench are connects to the source electrode, not to the gate conductive material.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5, lines 2-3, recites: a second trench adjacent to the first trench, the **second trench** including a conductive material coupled to the conductive material in the first trench.

By reciting "the first trench", the limitation is directed to the transistor structure, however, the conductive material of the transistors are independent from each other, no connection between the conductive material in the first trench and the second trench.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-8 and are rejected under 35 U.S.C. 103(a) as being unpatentable over Sapp (U.S. Patent No. 6,351,018) in view of X. Cheng et al. *Fast Reverse Recovery Body Diode in High-Voltage VDMOSFET Using Cell-Distributed Schottky Contacts*, both of record.

With respect to claim 1, as best understood by the examiner, Sapp teaches a monolithically integrated structure combining a field effect transistor and a Schottky structure (306) in an active area of a semiconductor substrate substantially as claimed, wherein:

the field effect transistor comprises:

a first trench (300-1) extending into the substrate and including a conductive material (302) forming a gate electrode of the field effect transistor; and

a pair of doped source regions (n+) positioned adjacent to and on opposite sides of the trench (300-1) and inside a doped body region, the doped source regions (n+) forming a source electrode of the field effect transistor, and the substrate forming a drain electrode of the field effect transistor, and

the Schottky structure (210) comprises:

a pair of adjacent trenches (300-3; 300-4) extending into the substrate, the pair of adjacent trenches (300-3; 300-4) including a conductive material (302) which is separated from trench side-walls by a thin layer of dielectric; and

a Schottky diode having a barrier layer formed on the surface of the substrate and between the pair of adjacent trenches (300-3; 300-4);

wherein the Schottky structure consumes a portion of the active area, and the field effect transistor consumes the remaining portion of the active area. (See Figs. 2-7).

Thus, Sapp is shown to teach all the features of the claim with the exception of explicitly disclosing a specific percentage of area occupied by the Schottky structure.

Sapp further teaches: [S]ince the area of the Schottky diode determines it forward voltage drop in response to current, Schottky structures with different numbers of adjacent trenches can be devised to arrive at the desired area. (See col. 5, lines 3-6).

Within purview of one having ordinary skill in the art, guided by the teaching of Sapp, it would have been obvious to determine the optimum area occupied by the Schottky diode. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation". Father, Applicant clearly admitted that "a ratio of the total area of the Schottky structure to the total area of the MOSFET in the range of 2.5% to 5% results in optimum performance". (See page 6, lines 24-26).

However, Cheng teaches a monolithically integrated structure combining a field effect transistor and a Schottky structure in an active area of a semiconductor substrate, the Schottky

diode occupies between 0% to more than 50% of the active area, (see Fig. 3 and Text), which is encompassed the claimed range 0.5-4.5%.

Note that the specification contains no disclosure of either the *critical nature of the claimed Schottky structure consumes 0.5-4.5%* of active area of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the monolithically integrated structure of Sapp having an optimized active area consumes by the Schottky structure as taught by Cheng to enhance the performance characteristic of the MOSFET switch, since such a modification would have involved a mere optimization of the total area consumes by the Schottky diode of Cheng.

Thus, within purview of one having ordinary skill in the art, guided by the teaching of Sapp and Cheng, it would have been obvious to determine the optimum area consumes by the Schottky structure. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover **optimum or workable ranges** by routine experimentation".

With respect to claim 2, the field effect transistor of Sapp further comprises a metal layer contacting the pair of doped source regions (n+), the metal layer and the barrier layer comprise one of either titanium tungsten or titanium nitride.

With respect to claim 3, the barrier layer and the metal layer of Sapp contacting the source regions (n+) connect together by an overlying layer of metal. (See Fig. 3).

With respect to claim 4, the barrier layer of Sapp forms the Schottky diode anode (304) terminal and the substrate forms the Schottky diode cathode terminal.

With respect to claim 5, as best understood by the examiner, the integrated structure of Sapp further comprises a second trench (300-2) adjacent to the first trench (300-1), the second trench (300-2) including a conductive material (302) coupled to the conductive material in the pair of the adjacent trenches, wherein a distance between the first trench (300-1) and the second trench (300-2) is greater than a distance W separating the pair of adjacent trenches (300-3; 300-4), and wherein the barrier layer and a metal layer contacting the source regions (n+) of the field effect transistor comprise one of either titanium tungsten or titanium nitride.

With respect to claim 6, as best understood by the examiner, the conductive material in the second trench (302-2) of Sapp electrically connects to the conductive material (302) in the pair of adjacent trenches (300-3; 300-4) between which the Schottky diode is formed. (See Fig. 3).

With respect to claim 7, the conductive material of Sapp in the pair of adjacent trenches (300-3; 300-4) between which the Schottky diode is formed is electrically isolated from the conductive material (302-1) in the first trench (300-1).

With respect to claim 8, the conductive material of Sapp in the pair of adjacent trenches between which the Schottky diode is formed, is recessed into the pair of adjacent trenches and covered by a layer of dielectric material. (See Fig. 4).

7. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sapp '018 and Cheng et al. as applied to claim 1 above, and further in view of Hurst et al. (U.S. Patent No. 6,437,386) of record.

Sapp teaches a monolithically integrated structure as described in claim 1 above including a first trench (300-1) extending into the substrate, wherein an insulating layer formed lining the side and bottom of the first trench.

Thus, Sapp is shown to teach all the features of the claim with the exception of the thickness of the insulating layer of the first trench as well as the pair of adjacent trenches along the bottom is thicker than that along the sidewalls.

However, Hurst teaches dielectric layer formed along the bottom (27) of a trench is thicker than that formed along the sidewalls (21) substantially reduces gate charge to reduce gate-to-drain capacitance thereby increasing the efficiency and prolong the life of the semiconductor device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the insulating layer lining the trenches of Sapp thicker on the bottom than on the sidewalls as taught by Hurst to reduce gate-to-drain capacitance thereby increasing the efficiency and prolong the life of the semiconductor device.

8. Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sapp '018 in view of Baliga (U.S. Patent No. 5,998,833) and Cheng et al., all of record.

With respect to claim 13, as best understood by the examiner, Sapp teaches a monolithically integrated structure combining a field effect transistor and a Schottky structure (210) in an active area of a semiconductor substrate (202) substantially as claimed, wherein:

the field effect transistor comprises:

a first trench (200-2) extending into the substrate;

a second conductive material (206) forming a gate electrode in the first trench (200-1);

a pair of doped source regions (212) positioned adjacent to and on opposite sides of the first trench (200-2) and inside a doped body region (214), the doped source regions (212) forming a source electrode of the field effect transistor, and the substrate forming a drain electrode of the field effect transistor, and

the Schottky structure (210) comprises:

a pair of adjacent trenches (200-3; 200-4) extending into the substrate (202), each pair of adjacent trenches (200-3; 300-4) including a conductive material (206); and

a Schottky diode (210) having a barrier layer (218) formed on the surface of the substrate (202) and between the pair of adjacent trenches (300-3; 300-4);

wherein the Schottky structure (210) consumes a portion of the active area, and the field effect transistor consumes the remaining portion of the active area. (See Figs. 2).

Thus, Sapp is shown to teach all the features of the claim with the exception of explicitly disclosing a first conductive material forming a shield electrode formed in the bottom and separated from the second, upper conductive material and a specific percentage of area occupied by the Schottky structure.

However, Baliga teaches the field effect transistor can be alternatively made including:

a first trench (20) extending into the substrate (10);

a first conductive material (26) forming a shield electrode in the bottom portion of the trench (20);

a second conductive material (30) forming a gate electrode in the trench (20), the second conductive material (30) being over but insulated from the first conductive material (26). (See Fig. 4H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the field effect transistor of Sapp including two separate conductive materials filling the trench as taught by Baliga to reduce the gate-to-drain capacitance and improve switching speed.

With respect to claim to the specific area occupied by the Schottky structure, Sapp further teaches: [S]ince the area of the Schottky diode determines it forward voltage drop in response to current, Schottky structures with different numbers of adjacent trenches can be devised to arrive at the desired area. (See col. 5, lines 3-6).

Within purview of one having ordinary skill in the art, guided by the teaching of Sapp, it would have been obvious to determine the optimum area occupied by the Schottky diode. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation". Father, Applicant clearly admitted that "a ratio of the total area of the Schottky structure to the total area of the MOSFET in the range of 2.5% to 5% results in optimum performance". (See page 6, lines 24-26).

However, Cheng teaches a monolithically integrated structure combining a field effect transistor and a Schottky structure in an active area of a semiconductor substrate, the Schottky diode occupies between 0% to more than 50% of the active area, (see Fig. 3 and Text), which is encompassed the claimed range 0.5-4.5%.

Note that the specification contains no disclosure of either the *critical nature of the claimed Schottky structure consumes 0.5-4.5%* of active area of any unexpected results arising therefrom. Where patentability is aid to based upon particular chosen dimension or upon another variable recited in a claim, the Applicant must show that the chosen dimension are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the monolithically integrated structure of Sapp having an optimized active area consumes by the Schottky structure as taught by Cheng to enhance the performance characteristic of the MOSFET switch, since such a modification would have involved a mere optimization of the total area consumes by the Schottky diode of Cheng.

Thus, within purview of one having ordinary skill in the art, guided by the teaching of Sapp and Cheng, it would have been obvious to determine the optimum area consumes by the Schottky structure. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover **optimum or workable ranges** by routine experimentation".

With respect to claim 14, the field effect transistor of Sapp further comprises a metal layer (216) contacting the pair of doped source regions (212), the metal layer (216) and the barrier layer (218) comprise one of either titanium tungsten or titanium nitride.

With respect to claim 15, the barrier layer (218) and the metal layer (216) contacting the source regions (212) connect together by an overlying layer of metal.

With respect to claim 16, the barrier layer (218) of Sapp forms the Schottky diode anode terminal and the substrate (202) forms the Schottky diode cathode terminal.

With respect to claim 17, in view of Baliga, the monolithically integrated structure of Sapp further includes: a second trench (200-1) adjacent to the first trench (200-2), the second trench including (as discussed above) a third conductive material (26) forming a shield electrode and a fourth conductive material (30) forming a gate electrode over but insulated from the third conductive material (26), wherein a distance between the first trench (200-2) and the second trench (200-1) is greater than a distance W separating the pair of adjacent trenches (200-3; 200-4), and wherein the barrier layer (218) and a metal layer (216) contacting the source regions (212) of the field effect transistor comprise one of either titanium tungsten or titanium nitride.

With respect to claim 18, in view of Baliga, the lower sidewalls (20a) and bottom (20b) of the first trench (20) is lined with a shield dielectric, and upper sidewalls (28) of the first trench (20) are lined with a gate dielectric, the shield dielectric (20a, 20b) being thicker than the gate dielectric (28).

Response to Arguments

9. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER